

DAVE McLELLAN

davemclellan@dmcldesigns.com

Senior Circuit Board Designer

SUMMARY

Skilled Printed Circuit Designer and CAD Librarian with over 30 years of circuit board design experience, including 17 years using Cadence Allegro and the SPECTRA auto-router capturing Concept and OrCad schematics in Windows and UNIX environments.

Accomplished designer of multi-layer fine-pitch, ball grid and standard surface-mount, as well as thru-hole technology. I have an enthusiastic attitude, with the ability to design independently or in a team environment. I also have well-developed organization and documentation skills and a strong mechanical design background.

ACCOMPLISHMENTS

Printed Circuit Design

- 17 years experience using Cadence Allegro in Windows and UNIX environments with current working knowledge of Allegro 16.1.
- Designed complex PC board layouts meeting engineering project schedules, integrating the latest design and manufacturing standards and implementing time reduction and cost savings practices.
- Created designs using Cadence Concept and OrCad schematic capture programs.
- Used SPECTRA auto-router to significantly reduce design time required on very dense circuit boards.
- Generated finished drawings detailing fabrication and assembly instructions on CAD system or by hand using mechanical design skills.
- Coordinated and expedited prototype manufacturing of circuit boards with various manufacturing and assembly companies, providing all required output files and information.
- Researched, developed and tested PC design tools, procedures, operations and methods and trained, instructed and directed employees resulting in increased overall efficiency of the department.
- Created and maintained web-based (HTML) ISO 9001 documentation detailing circuit design and department procedures.
Including: Step-by-step procedures for design preparation, design post processing, fabrication and assembly drawing standards and training references for contract designers.

CAD Librarian

- Created and managed Cadence "Allegro" and Intergraph "IEDS" PC board component libraries, combining printed circuit and mechanical design skills to research, create and document all thru-hole and surface-mount library parts, their associated pin/pad libraries for use by all company circuit designers.
- Created and maintained all library documentation, including: written procedures, part symbol catalogs, spec sheet catalogs and aperture files so any information regarding library symbols is easily accessible by the design department.
- Developed library standards for Cadence and Intergraph CAD systems, serving as librarian and as a member of standards committees during data base development on each system, evaluating and verifying that library creation decisions would provide reliable solutions for future tool upgrades and enhancements.
- Responsible for library file maintenance and backup, development and implementation of symbol checking and verification procedures to ensure that the library database met all quality standards and was fully protected.
- Created mechanical fabrication and assembly detail libraries for use by all designers on manufacturing drawings, using mechanical design background to develop precise instructional diagrams.

PROFESSIONAL EXPERIENCE

GRASS VALLEY GROUP/TEKTRONIX/THOMSON, Nevada City, CA **1974-2008**
Senior Circuit Board Designer, CAD Librarian, Mechanical Draftsman with abilities in Auto-Cad, Pro-E and Solid Edge. Graphic Artist, Web Page Designer, Technical Illustrator using Adobe Illustrator, PhotoShop, In-Design, HTML and CorelDraw.

Mechanical Draftsman **1972 - 1974**
ARISTOCRAT TRAILERS, Morgan Hill, CA
GRANGER ASSOCIATES, Menlo Park, CA
KAISER PERMANENTE, Cupertino, CA

EDUCATION/TRAINING

High School Graduate - Mountain View, CA - 2 years Mechanical Drafting
Foothill Junior College - Los Altos, CA - 1 year Mechanical Drafting

Company Sponsored Training including:

- Ball Grid Array Design
- Cooper and Chyan Technology Auto-Routing (SPECTRA)
- EMI and High Speed Design
- Controlled Impedance Design